

**IN THE CLAIMS:**

Please amend claims 1 and 5 as follows.

1. (Currently Amended) A method for controlling a phase locked loop during change of synchronisation source, ~~in which~~ wherein a fixed setting value of the phase difference is originally set for the phase locked loop, the method comprising:

[-] changing a synchronisation signal ~~is changed~~ from a first synchronisation to a second synchronisation signal;

[-] measuring a phase difference between said second synchronisation signal and a signal formed ~~from in~~ a phase lock's oscillator ~~is measured~~;


comparing the measured phase difference to a predetermined limit value;

[-] when the comparing step shows that the measured phase difference is greater than the predetermined limit value, changing the phase difference between the second synchronisation signal and the signal formed from the phase lock's oscillator ~~is changed, if a measured phase difference is greater than a predetermined limit value, whereupon the phase difference between said second synchronisation signal and the signal formed from the phase lock's oscillator is again measured~~;

[-] ~~the phase locked loop's normal adjustment function is started, when~~ repeating the measuring and comparing steps until the measured phase difference is less than or equal to a said predetermined limit value; and

~~wherein~~

~~in response to a finding that said~~ when the comparing step shows that the measured phase difference is less than or equal to said predetermined limit value, setting the measured phase difference is set as a new setting value for the phase difference for use in the normal adjustment function of the phase locked loop, whereupon the adjustment function is started instead of the fixed setting value.

 2. (Previously Presented) The Method method as defined in Claim 1, wherein phase transfer of the second synchronisation signal is carried out by preventing for a certain time access of the signal formed from the phase lock's oscillator to a component measuring the phase difference of the phase locked loop.

3. (Previously Presented) The Method method as defined in Claim 2, wherein preventing takes place by cutting off a functional route of the signal formed from the oscillator to the component measuring the phase difference of the phase locked loop.

4. (Previously Presented) The Method method as defined in Claim 2, wherein preventing takes place by cutting off ~~the~~ a functional route of the second synchronisation signal to the component measuring the phase difference of the phase locked loop.

5. (Currently Amended) A digital phase lock arrangement, ~~which includes,~~ comprising:

[-] selection components ~~for selecting~~ configured to select a desired synchronisation source from a set of at least two different synchronisation sources;

[-] a phase comparator, ~~which has~~ having a first and a second input ~~and which is used for generating~~ , configured to generate an output signal dependent on a phase difference between signals supplied to the inputs;

[-] controllers ~~for forming~~ configured to form a control word in response to an output signal which is dependent on the phase difference; and

[-] an oscillator, which is controlled with the aid of said control word;

wherein

said controllers ~~also include~~ comprising setting components ~~for setting~~ configured to set a measured phase difference as a new setting value for a normal adjustment function of a the phase lock arrangement instead of a fixed setting value of the phase difference originally set for the arrangement.

6. (Previously Presented) The Arrangement arrangement as defined in Claim 4, which includes starting components for starting the normal adjustment function of the loop, wherein said starting components respond to the setting components in order to start the adjustment function in response to a setting of a setting value.

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